REMARKS

The Office Action dated April 23, 2003 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. Accordingly, claims 1-7 are pending in this application and are submitted for consideration.

Entry of this Amendment is proper under 37 C.F.R. § 1.116 since this Amendment: (a) places the application in condition for allowance for reasons discussed herein; (b) does not raise any new issue regarding further search and/or consideration since the Amendment amplifies issues previously discussed throughout prosecution; (c) does not present any additional claims without canceling a corresponding number of finally-rejected claims and (d) places the application in better form for appeal, should an appeal be necessary. The Amendment is necessary because it is made in reply to arguments raised in the rejection. Entry of the Amendment is thus respectfully requested.

Applicants respectfully acknowledge the courtesies extended to Applicants' representative during the August 19, 2003 telephonic interview. During the interview, the Examiner agreed that the doping arrangement of Togei would not apply to the teaching of the prior art and stated that the Applicants arguments overcame the outstanding rejection of claims 1-7. The points discussed during the interview are incorporated herein.

Claims 1-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Applicants' Admitted Prior Art (AAPA) in view of Togei (U.S. Patent No. 4,247,863).

In making this rejection, the Office Action took the position that the AAPA

discloses all the elements of the claimed invention, except for disclosing the semiconductor region of the first conductivity type has an equal concentration of impurity as that of the semiconductor device. Togei is cited for curing the deficiencies of the AAPA. However, Applicants respectfully submit that claims 1-7 recite subject matter that is neither disclosed nor suggested by any combination of the prior art.

Claim 1 recites a semiconductor device that includes a lightly doped semiconductor substrate of a first conduction type, a buried semiconductor layer of a second conduction type, a semiconductor region of the second conduction type, and a semiconductor region of the first conduction type. The buried semiconductor layer is formed in a first region of the semiconductor substrate, spaced from a surface of the semiconductor substrate. The semiconductor region of the second conduction type extends from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer and is connected to the buried semiconductor layer. The semiconductor region of the first conduction type is formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type. The semiconductor region of the first conduction type is isolated from the semiconductor substrate by the buried semiconductor layer and the semiconductor region of the second conduction type. A concentration of an impurity in the semiconductor region of the first conduction type is equal to a concentration of an impurity in the semiconductor substrate

As a result of the claim configuration, the semiconductor region of the first conduction type is surrounded by the buried semiconductor layer of the second conduction type and the semiconductor region of the second conduction type. Thusly,

the semiconductor region of the first conduction type is isolated from the substrate by the buried semiconductor layer of the second conduction type and the semiconductor region of the second conduction type. Since the semiconductor region of the first conduction type is isolated from the substrate, an advantage is obtained that it is possible to apply a voltage to the semiconductor region of the first conduction type, which is lower than a ground voltage of the semiconductor substrate.

In the present invention, a concentration of an impurity in a semiconductor region of a first conduction type is equal to a concentration of an impurity in a semiconductor substrate. In the present invention, the semiconductor region of the first conduction type is not implanted with the impurity ion. Therefore, in the present invention, the semiconductor region of the first conduction type is not damaged by the impurity ion implantation.

Consequently, in the present invention, a leak current from a capacitor of a memory cell through a junction between a source/drain diffused layer and the semiconductor region is small, and frequent rewriting operations for retaining a charge of the capacitor are not necessary, whereby the semiconductor device can have small electric consumption.

As shown in Fig. 1, Togei discloses a semiconductor substrate 1, an insulating region 4, an N-type buried layer 2 buried in the semiconductor substrate 1, an N^+-type input-output region 5 connected to the electrode 12 connected to a bit line, and a P^+-type region 8 connected to a controlling electrode 11 connected to a word line. In Togei, when a reverse bias voltage is applied to the controlling electrode 11, a depletion layer will spread until it reaches the N-type buried layer 2. Accordingly, a punch-through

effect is realized in the substrate 1 between the N^+-type input-output region 5 and the N-type buried layer 2. Due to the punch-through effect, information is written into the N-type buried layer 2 and the information is read out of the N-type buried layer 2. (See col. 3, lines 23-30)

As shown in Fig. 3, in Togei, the N-type buried layer 2 is in contact at its peripheral end with the insulating region 4. In Togei, since the N-type buried layer 2 is in contact with the insulating region 4, an electrical potential distribution in a P-type portion 1a is advantageously changed, and the punch-through effect is effectively realized. (See col. 4, lines 6-11)

In the Office Action, it was asserted that Togei teaches a semiconductor region of a first conductivity type (P-type portion 1a) surrounded by a buried semiconductor layer (N-type buried layer 2) surrounded by isolation region (4), wherein a concentration of an impurity in the semiconductor region of the first conduction type (1a) is equal to a concentration of an impurity in the semiconductor substrate (1). The Office Action cited col. 2, lines 30-66 and col. 4, lines 3-45 in support of this assertion. It was therefore concluded that it would have been obvious to modify the AAPA with Togei in order to improve speed due to effective movement of carriers.

However, firstly, in Togei, the N-type buried layer (2) is for storing information and the N-type buried layer (2) acts as a capacitor of a memory device. On the other hand, an n-well (138) of the AAPA is for isolating a p-well (164) from a semiconductor substrate (114). The reason that the p-well (164) is isolated from the semiconductor substrate (114) is for supplying a voltage Vbb lower than a ground voltage Vss of the semiconductor substrate (114) to the p-well (164).

Secondly, in Togei, the reason that the N-type buried layer (2) is in contact with the insulating region (4) is for changing the electrical potential distribution in the P-type portion (1a) advantageously and so that the punch-through effect can be realized effectively. On the other hand, in the AAPA, the reason that the p-well (164) is surrounded by the n-well (138) is for isolating the p-well (164) from the semiconductor substrate (114).

Thirdly, in Togei, the insulation region (4) is made of silicon oxide. In Togei, the insulation region (4) is not made of n-type semiconductor. On the other hand, in the AAPA, n-well (138) is made of n-type semiconductor. Therefore, in Togei, it is impossible to use the n-type semiconductor as the insulation region (4). In Togei, if the n-type semiconductor is used as the insulation region (4), the N^{+}-type input-output region (5) and the N-type buried layer (2) are electrically connected to each other by the region (4), and consequently, the N-type buried layer (2) cannot function as the capacitor of the memory device.

Lastly, in Togei, the P-type portion (1a) and the silicon substrate (1) are not connected to different voltages. On the other hand, in the AAPA, the p-well (164) and the semiconductor substrate (114) are connected to different voltages. That is, in the AAPA, the p-well (164) is connected to the voltage Vbb lower than a ground voltage Vss of the semiconductor substrate (114). The reason that the p-well (164) is connected to the voltage Vbb lower than the ground voltage Vss of the semiconductor substrate (114) is raising a threshold voltage of a transistor (148) formed on the p-well (164).

Therefore, as discussed above, Applicants submit that the AAPA and Togei, either alone or in combination, fail to disclose or suggest the claimed invention, and it is

respectfully submitted that the Applicants' invention, as set forth in claim 1 is not obvious within the meaning of 35 U.S.C. § 103.

Still further, because claims 2-7 are dependent on claim 1 , Applicants submit that that these claims recite subject matter that is neither disclosed nor suggested by the cited prior art, for at least the reasons set forth above with respect to claim 1 .

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1-7, and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108077-08003.**

Respectfully submitted,

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